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Innovation by Lam Research, a Semiconductor Equipment Manufacturer - Lam Research's Breakthrough in the Japanese Oxide Etcher Market -

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Abstract:

In 2004, there was a dynamic change of market share in the Japanese semiconductor equipment industry. More specifically, there was a dramatic increase in the market share held by Lam Research Corporation in the Japanese market for silicon oxide dry etching equipment ('etcher' for short).

The reason Lam Research, previously a minor player in the Japanese oxide etcher market, was able to achieve such an increase in market share is explained as follows. The semiconductor industry was faced with a transition in technologies such as diameter of silicon wafers and material of metal and dielectric films, thereby creating a need for new oxide etchers. At this time, Lam Research succeeded in developing a new oxide etcher with superior productivity. Marketing strategy by Lam Research Japan also contributed significantly to increasing the market share.

Lam Research's advancement was further propelled by its breakthrough in the long-practised oxide dry etching technology, in other words, an innovation. This innovation by Lam Research was made possible by its corporate policy.

Acknowledgment

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1. Introduction

There is a semiconductor manufacturing equipment business associated with the semiconductor chip industry. This paper focuses on the market share competition by dry etching equipment manufacturers in one part of this equipment business. Dry etching equipment is called 'etcher' for short in this paper.

Dry etching is a semiconductor processing technology that uses plasma to make fine patterns such as via holes and trenches. There are three kinds of etchers available, each for processing different materials: gate (silicon), metal (aluminium and tungsten) and silicon dioxide (SiO_2, hereinafter 'oxide'). The ratio of the three etchers at a standard semiconductor factory is 20% for gate, 10% for metal wiring and 70% for oxide [1]. The ratio of oxide etcher is the largest, and for this reason, etcher manufacturers make a great effort to gain a larger market share in the oxide etcher market.

Since 1990, Tokyo Electron Limited (TEL) has held the largest market share in the oxide etcher market. In the recent years, TEL has enjoyed a share of 70% and 80% in the world market and the Japanese market, respectively (Fig. 1 and 2). On the contrary, market share held by Lam Research was about 10% in the world market and several percent at most in the Japanese market [2].

However, Lam Research's market share rose sharply through the years 2003-4. Their market share increased 2.5 times in the world market from 10 to 25%, and more than 6 times from 3 to 20% in the Japanese market [3]. In particular, Lam Research was able to obtain about a third of the market share for oxide etchers for 12-inch wafers (Fig. 3), and almost a half of the market share for oxide etchers for Cu/Low-k (Fig. 4) [4] [5].

How was Lam Research, which had long trailed far behind in the Japanese oxide etcher market, able to expand its market share so much over these years? This study intends to provide an answer to this question, as a result concluding that Lam Research was able to achieve an innovation in oxide dry etching technology.

In the following sections, dry etching technology is first explained, followed by an examination of why Lam Research was able to grow its market share in the Japanese

oxide etcher market. In summary, in 2003-4, the semiconductor industry was faced with a period of technological transition, which created a need for new oxide etchers. At this time, Lam Research developed a new oxide etcher with superior productivity. Marketing strategy by Lam Research Japan also contributed significantly to increasing the market share. Lam Research's advancement was propelled by its breakthrough in the long-practised oxide dry etching technology, in other words, an innovation. Finally, Lam Research's corporate policy is discussed as the driving force behind this innovation.

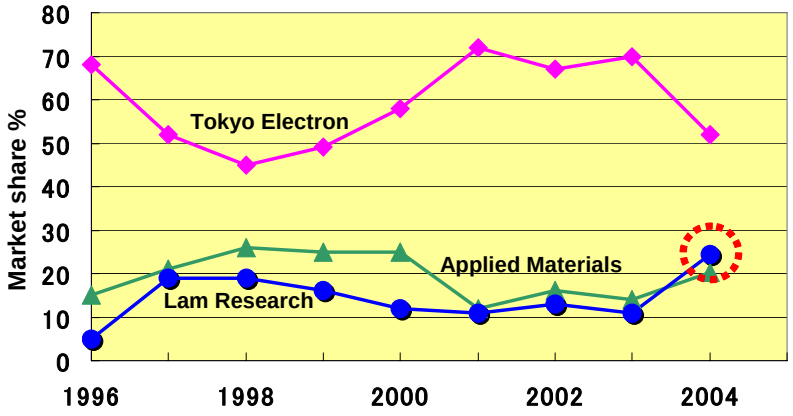

Fig.1 Oxide etcher market share in the world.

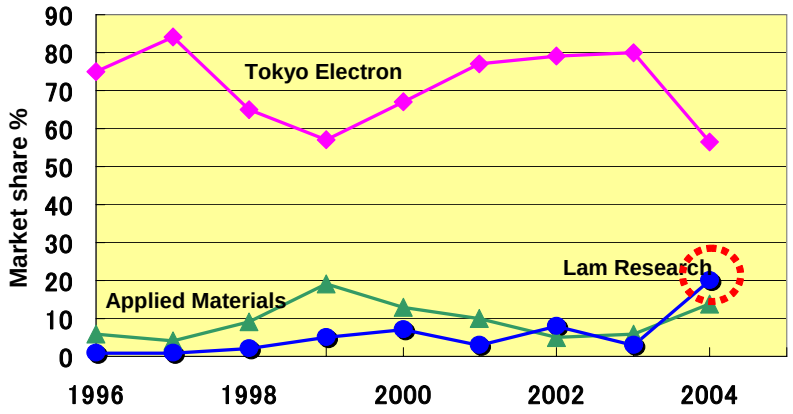

Fig.2 Oxide etcher market share in Japan.

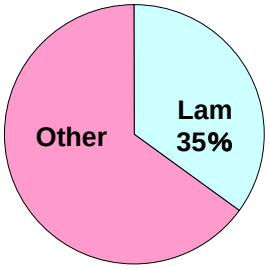

Fig. 3 Lam Research market share of oxide etcher for 12- inches wafer in Japan.

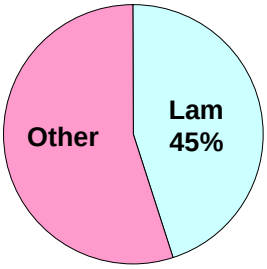

Fig. 4 Lam Research market share of the oxide etcher for Cu/ Low-k in Japan.

2. Dry etching technology

Dry etching is a fine processing technology by which a solid material, such as an oxide, is changed to volatile products (referred to as 'reaction products') by means of chemical reactions within a vacuum chamber with ions and radical species generated in plasma, and then exhausted.

Fig.5 illustrates the oxide dry etching process [6].

a) Radical species, such as -CFx (x=1-3), are generated in plasma of CF4 and Ar, and are adsorbed onto the oxide surface.

b) When ions, such as Ar^+, generated in plasma, collide with the oxide surface, the local temperature of the surface rises rapidly. This zone of high local temperature is called a 'hot spot'. The oxide reacts chemically with radical species of -CFx using the thermal energy of the hot spot.

c) Volatile reaction products such as SF4, CO and CO2 are generated by the chemical reaction. The oxide etching proceeds by evaporation of these reaction products.

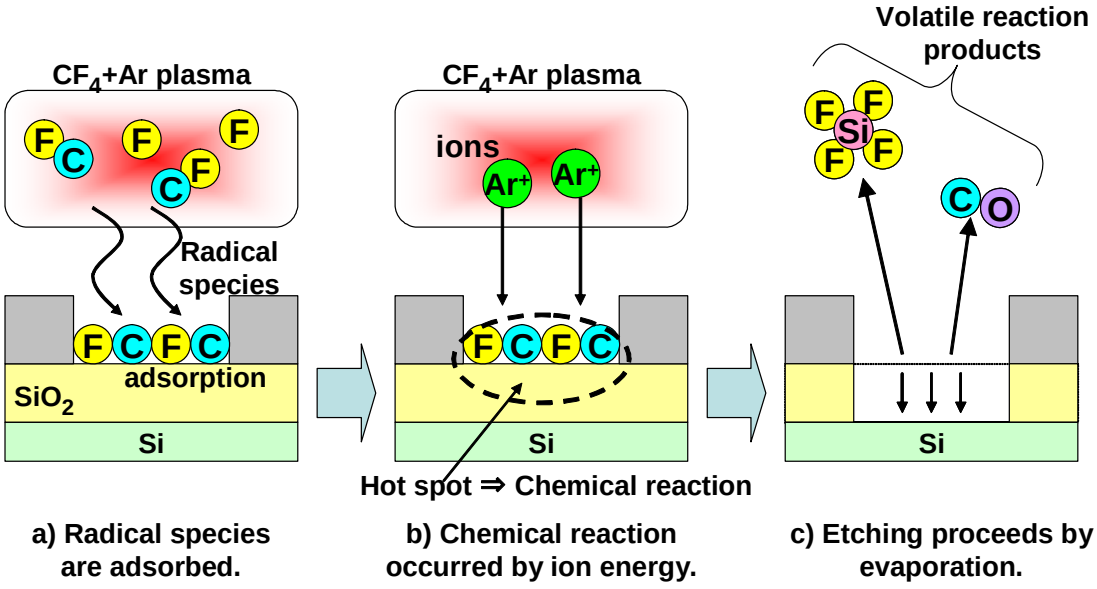

Fig.5 Mechanism of dry etching (case of SiO_2).

Just as road construction works generate gravel, dry etching for fine processing of via or trench produces reaction products. The difference is, while gravel is solid, reaction products are generated as gas.

The reaction products are exhausted with a vacuum pump. However, if the reaction

products collide with the inner wall of the vacuum chamber before they are exhausted, they turn back from gas to solid, and combine with radical species of -CFx to form polymers (hereinafter 'CF polymers') that are deposited onto the inner wall. This deposition may have an adverse effect on the dry etching process.

In a mass-production factory for semiconductor devices, a dry etcher must process several hundred silicon wafers each day. In the mass-production of semiconductor devices, it is essential that identical etching characteristics are achieved under identical etching conditions. It is also necessary to control the deposition of reaction products onto the inner wall, so as to maintain the stability of etching characteristics such as etching rate and uniformity. Lam Research developed a new oxide etcher with an epoch-making method for controlling the reaction products, the details of which are explained in section 4.

Section 3 discusses the years 2003-4, during which the oxide etcher market share of Lam Research grew, in terms of the history of semiconductor technology, the changes in semiconductor technology that took place during this transition period, and a new etcher that came into demand as a result.

3. Transition of semiconductor technology

Since the development of 1K bit DRAM and the 4004 processor by Intel in 1971, the number of transistors contained in an integrated circuit (IC) has increased four-folds every three years, in accordance with the Moore's law. At the same time, the size of transistors has shrunk by 70% every three years, in accordance with the scaling law. In the past 30 years, the integration degree of DRAM has been increased from 1K to 256M bit, with the minimum pattern size scaled down from 10 μm to 90 nm, as illustrated by Fig. 6.

With the increasingly high integration of semiconductor devices and the shrinking of transistors, semiconductor technology faced three major changes in 2003-4: 1) enlargement of wafer diameter from 8 to 12 inches; 2) transition of lithography technology from krypton fluoride (KrF) to argon fluoride (ArF); and 3) transition of metal and dielectric film from Al/SiO_2 to Cu/Low-k. This section explains these technological changes, as well as the need for a new kind of oxide etcher that resulted.

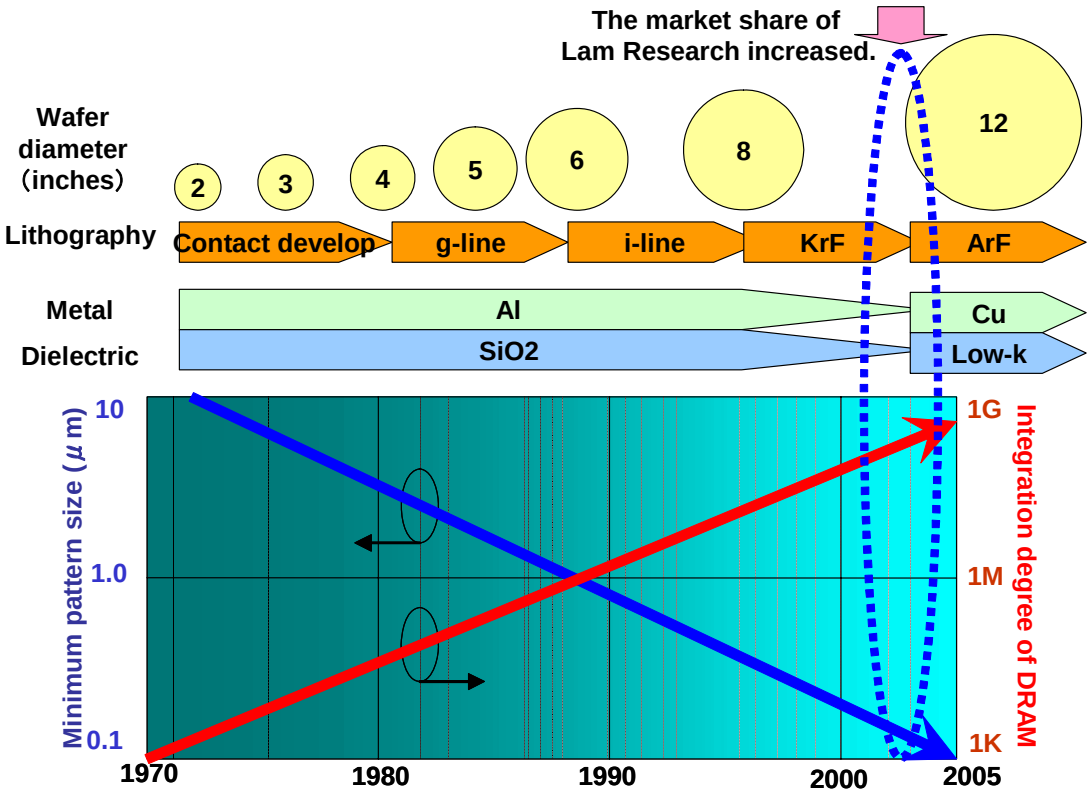

Fig.6 Semiconductor technology in transition.

3.1 Expansion of wafer diameter

Semiconductor chips are manufactured from silicon wafers. The cost of a semiconductor chip decreases as the number of chips manufactured from a single silicon wafer increases. Hence, there are two ways to lower the cost. One is to shrink the chip size. The other is to use wafers with a larger diameter. Over the past 30 years, the diameter of silicon wafer has gradually grown from 2 inches to 3, 4, 5, 6 and 8 inches, finally reaching 12 inches in 2004.

When the wafer diameter is expanded, existing semiconductor production equipments become useless as they cannot accommodate the silicon wafers with the expanded diameter. With the expansion of silicon wafer diameter from 8 inches to 12 inches, semiconductor production equipment for 8-inch wafers were made obsolete, creating an immediate need for equipment compatible with 12-inch wafers. Naturally, oxide dry etchers for 12-inch wafers also became needed, and this is what happened in 2003-4.

3.2 Transition of lithography technology

When processing the oxide film on a silicon wafer into fine patterns such as via holes and trenches, resist masks must first be formed by lithography, before dry etching can take place. Photo printing technology is applied in forming the resist masks. As such, there is a positive and a negative, just as with photography. Here, the formation of a positive resist mask, better suited for fine processing, is explained along with an example of fine patterning (Fig.7).

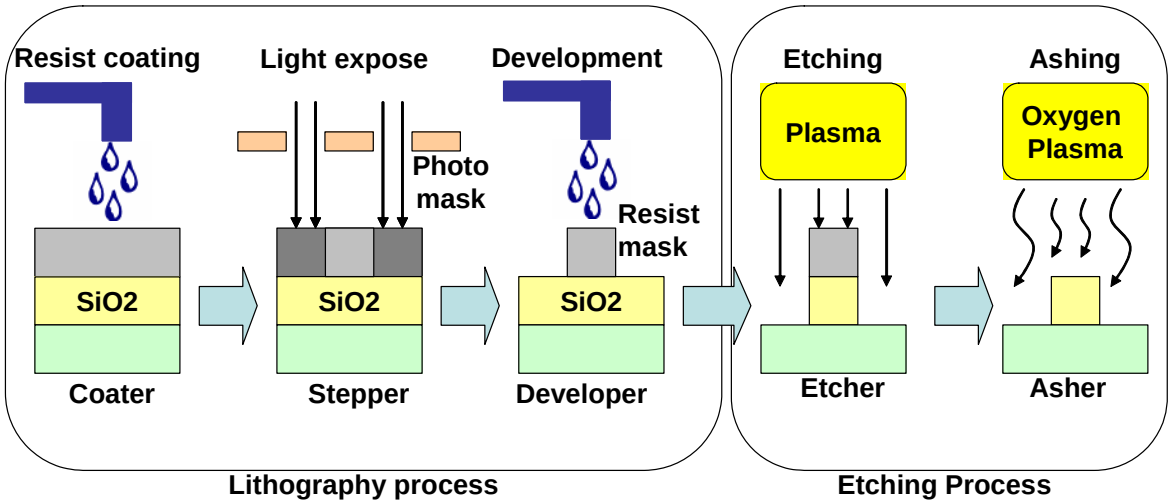

Fig.7 Fine processing technology.

First, oxide film deposited on the silicon wafer is coated with a photo-sensitive resist material, of which carbon is the primary ingredient. The resist material is then exposed to light through a photomask. The exposed resist material changes structure, becoming more fusible. When the silicon wafer is immersed in the developing fluid, the exposed parts dissolve and the unexposed parts remain, forming a resist mask on the oxide. Then, via holes and trenches are formed by dry etching. Finally, the resist mask no longer necessary is removed by ashing using oxygen plasma.

In order to process fine via holes and trenches, a fine resist mask is naturally required. To create a fine resist mask, exposure through the photomask must be performed with light with a shorter wave length, as shorter wave length improves resolution of the resist material. For this reason, the wave length of light sources used in lithography equipment has been shortened from white light to g-line (436 nm) and i-line (365 nm) of mercury lamps, and then to KrF excimer laser (248 nm). In 2004, ArF excimer laser (193 nm) was introduced [7] (Fig. 8).

With the change in light source from KrF to ArF, the resist material was also changed. The plasma tolerance of ArF resist is weaker than that of KrF resist. That is to say, ArF resist mask is also less vulnerable to etching by plasma. If the resist mask is damaged by etching, fine patterns cannot be formed. Hence, an oxide dry etching technology less likely to damage the ArF resist mask became necessary.

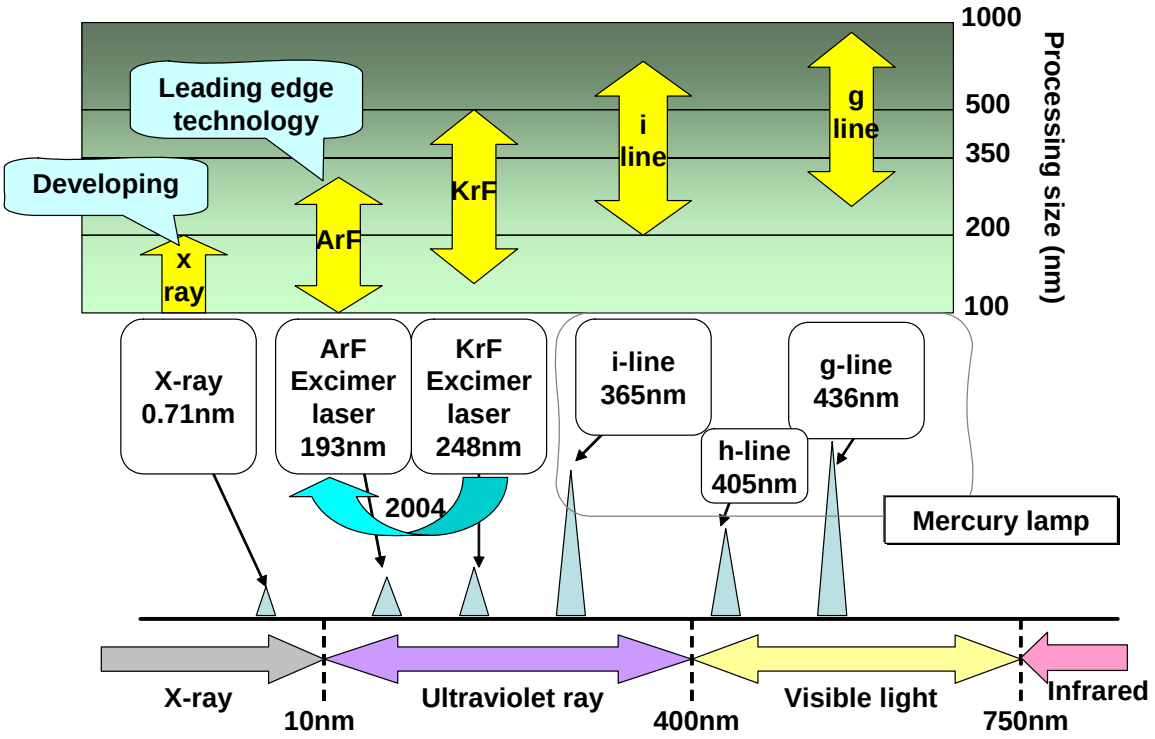

Fig.8 The wave length of light source for lithography has been shorted.

3.3 Transition of materials for metal and dielectric film

As previously mentioned, transistor size has been shrunk by 70% every three years for the past 30 years in accordance with the scaling law, so as to achieve higher performance of semiconductor devices, such as higher integration, lower power consumption and higher access speed.

However, it has become clear that the access speed of semiconductor devices decreases when the minimum pattern size becomes smaller than 130 nm (Fig. 9). When the transistor is shrunk according to the scaling law, the cross sectional area of the metal wiring is shrunk, as is the space between the wiring. As a result, resistance (R) and capacitance (C) for the wiring both increase, causing a signal delay (RC delay) on the semiconductor device [8].

To prevent this RC delay, metal with small R and dielectric film with low C are

required. To decrease the C, dielectric film with low relative dielectric constant (k) should be used. Such film is called a 'low-k' film. Until now, aluminium (Al) and SiO_2 have been used for the metal and the dielectric film, respectively. To satisfy the above requirement, however, copper (Cu) with low R and low-k film are now being used instead of Al and SiO_2.

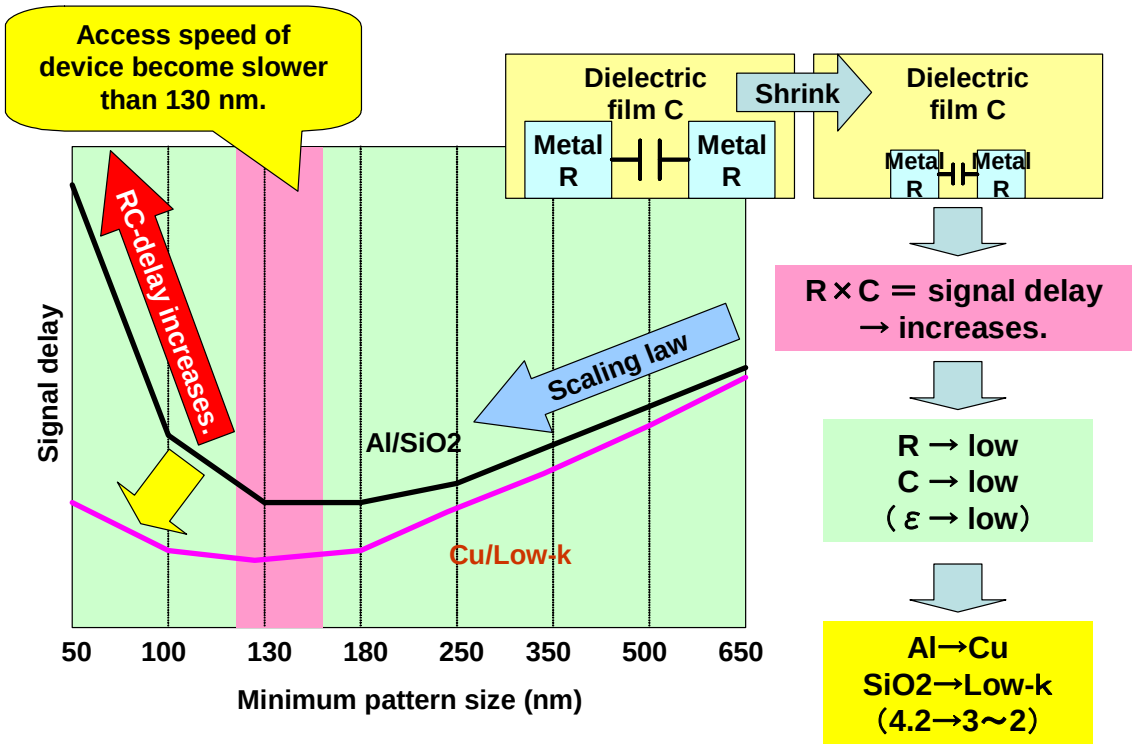

Fig.9 Cu and low-k film were needed for semiconductor devices.

Why is an oxide etcher, not a metal etcher, necessary for the Cu/Low-k interconnection process? The reason lies in the difference between the Al/SiO_2 process and the Cu/Low-k process. Al/SiO_2 interconnects are formed by actually dry etching the Al (Fig. 10(a)). On the other hand, due to the extreme difficulty in the dry etching of Cu, Cu/Low-k interconnects are formed in the following manner (Fig. 10(b)).

First, a low-k film is deposited. Resist masks are then formed on the low-k film by lithography. Trenches are made by dry etching of the low-k film. After the dry etching, resist masks are removed by ashing using oxygen plasma. The trenches are filled with Cu by electric plating. Finally, unwanted Cu is removed by chemical mechanical polishing (CMP).

This process is called 'damascene' [9]. In forming the Cu/Low-k interconnects, Cu is not etched, but the low-k film is etched instead. Hence, an oxide etcher becomes necessary for the processing of low-k films.

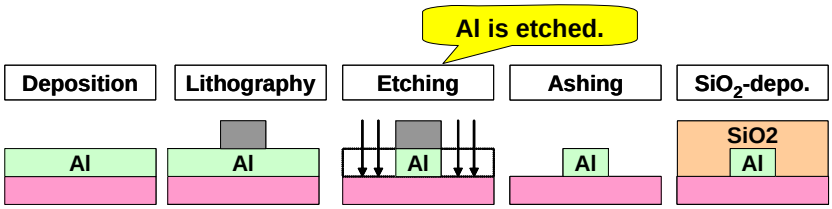

Fig.10(a) Al/SiO_2 process.

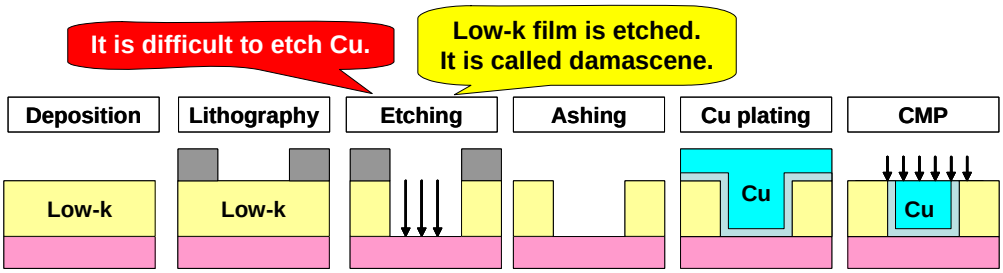

Fig.10(b) Cu/Low-k process.

3.4 Reduction of the process flow for Cu/Low-k interconnection

In using the damascene process for forming Cu/Low-k interconnects, there was a need to reduce the number of steps in the process flow. For this purpose, a process called 'dual-damascene' had to be realized. Dual-damascene is a process that forms the second Cu metal layer while simultaneously forming via holes that connect the first and second Cu metal layers.

A description of the dual-damascene process follows (Fig. 11) [9].

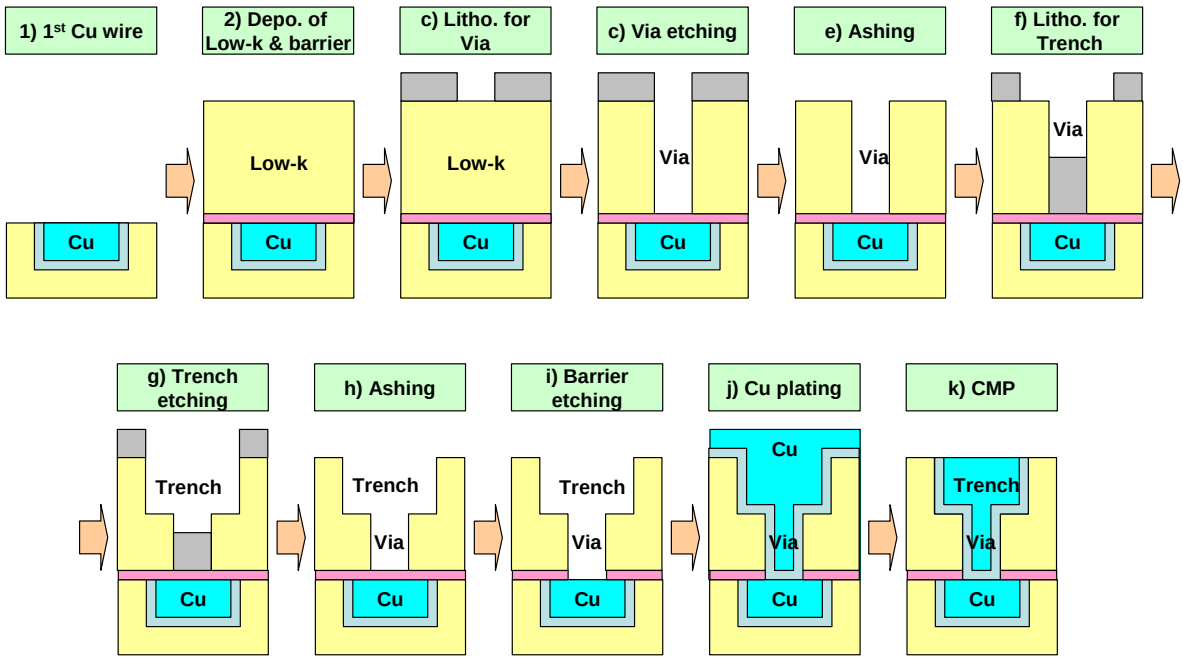

Fig.11 Dual-damascene process flow.

a) The first Cu metal layer is formed by single damascene.
b) Barrier film and low-k film are deposited onto the first Cu metal layer.
c) Resist mask for via holes is formed by lithography on the low-k film.
d) Via holes are formed by dry etching.
e) Resist mask is removed by ashing using oxygen plasma.
f) Resist mask for trenches is formed by lithography on the low-k film.
g) Trenches is formed by dry etching.
h) Resist mask is removed by ashing using oxygen plasma.
i) Barrier film is etched.
j) Via holes and trenches are filled with Cu by electric plating.
k) Unwanted Cu is removed by CMP.

As described, the dual-damascene process reduces the number of steps in the process flow by simultaneously forming via holes and trenches for Cu interconnects. This dual-damascene process was requested of the new generation of oxide etchers.

3.5 The need for new oxide etchers

Silicon wafers were expanded in diameter to 12 inches, lithography technology shifted from KrF to ArF, and metal and dielectric film switched from Al/SiO_2 to Cu/Low-k. As a result, there was a demand for new oxide etchers that support 12-inch wafers and Cu/Low-k processes. The new etchers were further required to realize oxide dry etching without erosion of ArF resist, as well as the dual-damascene process for the formation of Cu/Low-k interconnects.

Dry etcher manufacturers had to compete in their development of new oxide etchers and new technologies. What was Lam Research able to develop under such a situation?

4. Oxide etcher developed by Lam Research

The new oxide etcher developed by Lam Research was named '2300 Exelan® Flex™' (hereinafter 'Exelan') [10]. Section 4 focuses on the strong points of the Exelan, and on the etching technologies it realized.

4.1 Support for both 8- and 12-inch wafers

Lam Research developed an oxide etcher compatible with both 8- and 12-inch wafers. Moreover, their oxide etchers allow oxide dry etching conditions for 8-inch wafers to be converted into etching conditions for 12-inch wafers (Fig. 12). These characteristics enable the effective reuse of 8-inch wafer processes.

As a result, the technology transfer for semiconductor devices developed in R&D centres with 8-inch wafers to mass-production fabs using 12-inch wafers become much easier. Since there are many manufacturers who develop new processes in R&D centres with 8-inch wafers and mass-produce semiconductor chips in fabs with 12-inch wafers, this presents an extremely attractive advantage for many. It is also effective for saving expensive 12-inch wafers.

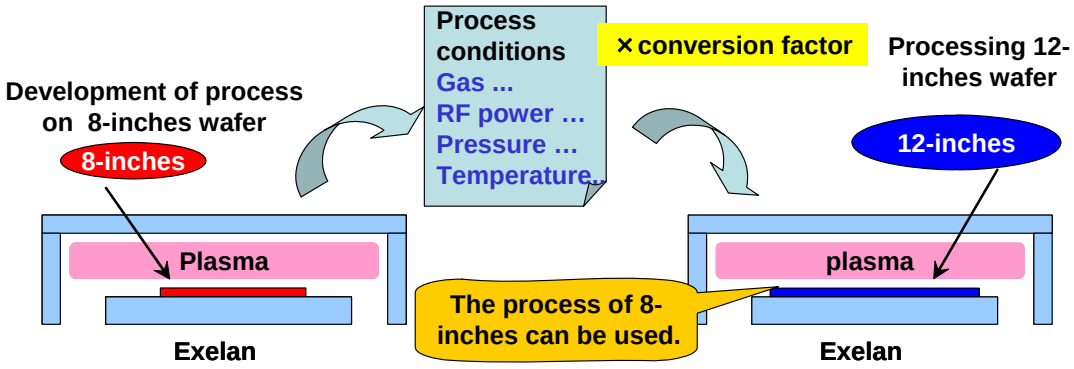

Fig.12 Exelan can etch both 8- and 12-inches wafer.

4.2 Controlling ion energy and reaction products

Lam Research developed a unique plasma confinement technology called 'Dual Frequency Confinement' (DFC^{TM}) [10]. This is an epoch-making technology for controlling ion energy and reaction products.

4.2.1 Control of ion energy

Lam Research's Exelan uses two RF power sources to simultaneously apply both high and low frequencies to the bottom electrode [11]. In general, plasma generated by an RF source with low frequency has a broad ion energy distribution function (IEDF), and always contain high energy ions. On the other hand, plasma generated by an RF source with high frequency has a sharp IEDF, and is more accepting to low energy ions.

By combining high and low frequencies, Lam Research succeeded in controlling a wider range of ion energy [11].

ArF resist is more prone to erosion by high energy ions. In order to perform etching without damaging the ArF resist, it is necessary to decrease the ion energy in the plasma. Exelan is capable of working around the low plasma tolerance of ArF resist, thanks to its ability to control a wide range of ion energy.

4.2.2 Control of reaction product

In the conventional oxide etchers, plasma touched the inner wall of the vacuum chamber. In Exelan, plasma is physically confined, and does not touch the inner wall of the chamber. This difference of whether or not plasma comes in contact with the inner wall is what makes Exelan so much more effective. It is where the true value of Lam Research's development lies.

(1) Reaction product control by conventional etchers

A conventional oxide etcher in which plasma touches the inner wall of the vacuum chamber will first be explained (Fig. 13(a)). As mentioned in Section 2, volatile reaction products are generated by dry etching. In this case, reaction products collide with the inner wall, turn solid, and form CF polymers that are deposited onto the inner wall. Even if CF polymers are deposited onto the inner wall, there is no problem if no particles are generated within the chamber.

If oxygen gas is introduced into the chamber deposited with CF polymers, however, the chamber wall material (Al), CF polymer and oxygen react chemically, generating a non-volatile substance (AlF). The non-volatile substance becomes particles (dust) for silicon wafers and decreases the 'yield', the ratio of quality semiconductor chips obtained from a wafer. This implies that oxygen gas cannot be introduced into the chamber, which means that resist-removal after dry etching, in other words the ashing by oxygen plasma, cannot be employed within the etching chamber. For this reason, until now, an exclusive ashing equipment (asher) had been used for the removal of resist by oxygen plasma.

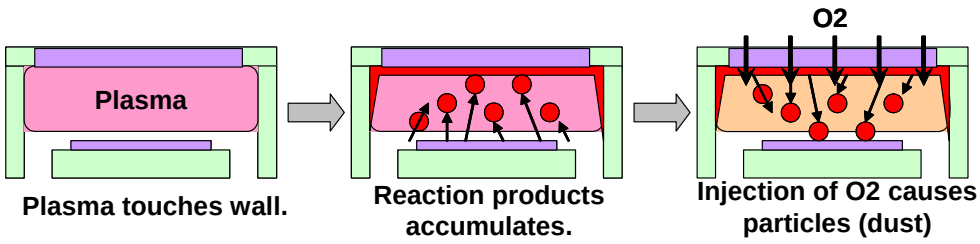

Fig.13(a) Reaction product control by the conventional oxide etcher in which plasma touches wall.

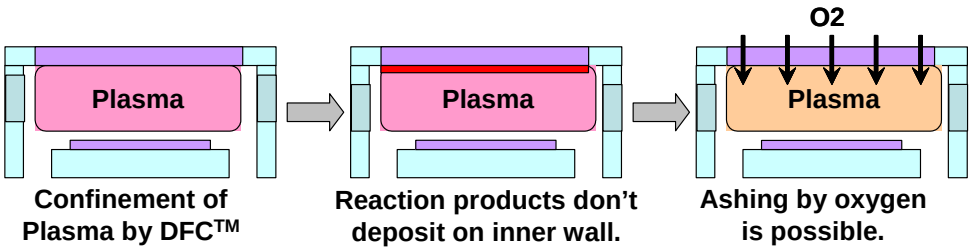

Fig.13(b) Reaction product control by confinement plasma of Exelan.

(2)Reaction product control by Exelan

Exelan controls reaction product as shown in Fig. 13(b). The plasma is physically confined by DFC™, so plasma does not touch the inner walls of the chamber, and reaction products such as CF polymer are not deposited onto the inner walls. Reaction products deposited on the top electrode are removed by cleaning using oxygen plasma. This means that no particles are generated, and allows for oxide dry etching and ashing to be performed consecutively within the same etching chamber.

(3) Cu/Low-k dual-damascene by Exelan

Exelan allows etching and ashing to take place consecutively within the etching chamber. This contributes to decreasing the number of steps in the dual-damascene process flow for Cu/Low-k interconnection.

In the case of a conventional etcher, the dual-damascene process flow for Cu/Low-k interconnection is as follows (Fig. 14(a)):

1) Resist mask for via holes is formed by a stepper.
2) Via holes are formed by an oxide etcher.
3) Resist mask is removed by an asher using oxygen plasma.
4) Resist mask for trenches is formed by a stepper.
5) Trenches are formed by an oxide etcher.
6) Resist mask is removed by an asher using oxygen plasma.
7) Barrier film is removed by an etcher.

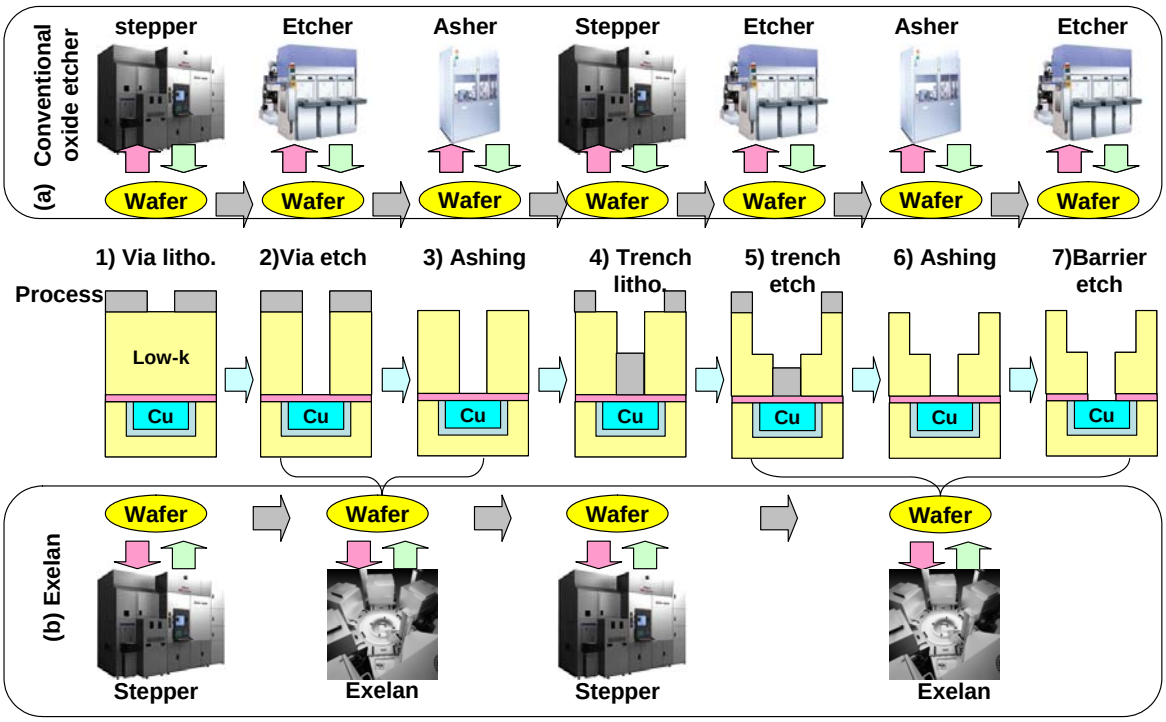

Fig.14 Dual-damascene by using conventional oxide etcher and Exelan.

In the case of Exelan, the dual-damascene process flow for Cu/Low-k interconnection is as follows (Fig. 14(b)):

1) Resist mask for via holes are formed by a stepper.
2) and 3) Etching of via holes and ashing of resist are processed consecutively by Exelan.
4) Resist mask for trenches is formed by a stepper.
5), 6) and 7) Etching of trenches, ashing or resist and etching of barrier film are processed consecutively by Exelan.

Exelan's application of dual-damascene for Cu/Low-k interconnection eliminates the need for an exclusive asher. It is no longer necessary for the silicon wafers to be returned to the etcher for barrier etching after ashing. The frequency of insertion/withdrawal of wafers into/from the etcher is decreased, and as a result, the generation of particles is reduced.

(4) Merits of Exelan

The introduction of Exelan to a semiconductor mass-production fab offers the following advantages over the use of a conventional etcher [10]. Each figure is

calculated with respect to a conventional oxide etcher.

a) Number of equipments is decreased to 60% (Fig. 15(a)).
b) Number of chambers is decreased to 70% (Fig. 15(b)).
c) Footprint of equipments is decreased to 50% (Fig. 15(c)).
d) Investment for equipments is decreased to 65% (Fig. 15(d)).
e) Cycle time required for the handling of wafers is decreased to less than 50% (Fig. 15(e)).

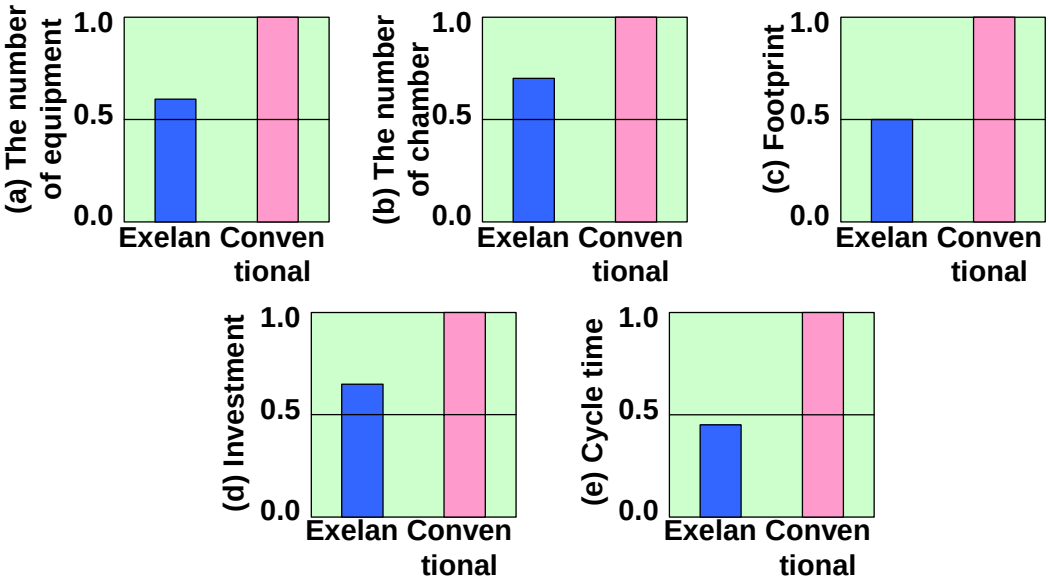

Fig.15 High performance of Exelan

In addition, the mean time between cleaning (MTBC), which is the number of days after which the equipment requires wet-cleaning, is increased by several folds. A certain factory was able to use Exelan for oxide etching for 90 consecutive days without cleaning [12].

In short, the use of Exelan prevents plasma from touching the inner walls of the chamber, enabling the consecutive processing of etching and ashing, thus leading to an extremely effective mass-productivity of semiconductor devices.

5. Marketing strategy by Lam Research Japan

As discussed, Lam Research succeeded in developing an extremely productive oxide etcher for 12-inch wafers and Cu/Low-k interconnects. What marketing strategy did Lam Research Japan employ to sell this new oxide etcher?

5.1 Situation of Lam Research Japan

During the years 2001-2, the semiconductor industry was suffering a big depression caused by the silicon cycle. Semiconductor manufacturers and related businesses were compelled to lay off many of their employees. Lam Research Japan being no exception was also forced to take downsizing measures, including the shut-down of their demonstration facilities [13]. As market conditions worsened, Lam Research Japan was driven into a corner [14].

However, the situation also made Lam Research Japan more slim and flexible as an organization. They were transformed into an organization with a ‘shallow’ and ‘lean’ structure, more capable of reflecting on the voices of the customers [14].

5.2 Sales of Lam Research Japan

With their restructured organization, Lam Research Japan carried out a ‘selection and concentration’ marketing strategy [14]. Having reduced the number of their employee to half, Lam Research Japan was unable to do business evenly with all Japanese semiconductor manufacturers. Instead, they selected several big players in the industry to do business with. Lam Research Japan put all sales effort and resources into these selected few. This marketing strategy went well. As a result, Lam Research Japan was able to sell a large number of their oxide etchers for 12-inch wafers and Cu/Low-k interconnects [15].

6. Innovation by Lam Research

Exelan was also successful as an etcher for non-Cu/Low-k uses [16]. This could be an implication of something more than Lam Research developing a highly productive oxide etcher and Lam Research Japan being effective in their 'selection and concentration' strategy. Lam Research had made a breakthrough with Exelan, and realized an innovation in the field of oxide dry etching technology. This innovation is discussed below.

6.1 Common sense in oxide dry etching technology

A certain 'common sense' in oxide etching technology was firmly established in the use conventional etchers in which plasma touches the inner walls. (Refer to Fig. 13(a)) [17].

a) A clean oxide etching chamber that has just been wet-cleaned.
b) A product wafer is etched using the chamber. Reaction products collide with the inner walls of the chamber, resulting in the deposition of CF polymers onto the inner walls.
c) As the number of etched product wafers increases, the amount of CF polymer deposited on the inner walls also increases. As illustrated by Fig. 13(a), ashing by oxygen plasma cannot be employed in the etching chamber, so etching of product wafers is continued with CF polymers deposited on the walls.
d) After a week of use, reaction products deposited on the inner walls of the etcher begin to fall. They become particles (dust) that worsen the yield.
e) Hence, before particles are generated, the oxide etcher must be shut down, and have the chamber opened and wet-cleaned to remove the reaction products deposited on its inner walls. After wet-cleaning, product wafers can once again be processed, and this work flow is repeated from step a).

In short, it was common sense that an oxide etcher must be cleaned at least once a week. Semiconductor manufacturers have practised this cycle for over fifteen years.

6.2 Breakthrough by Exelan

Lam Research's Exelan made a breakthrough to the above cycle, as described below (Refer to Fig. 13(b)).

a) A clean Exelan chamber that has just been wet-cleaned.
b) A product wafer is etched using the chamber. Plasma confinement technology (DFC^{TM}) prevents reaction products from being deposited onto the inner walls of the chamber.
c) Reaction products deposited onto the surface of the upper electrode are removed by cleaning using oxygen plasma.
d) As a result, product wafers can be processed in a clean chamber each and every time.
e) Oxide etching using DFC^{TM} and oxygen plasma cleaning allows processing of product wafers to continue for a duration that is several times longer than before.
f) After a consecutive operation extending over several weeks, the Exelan chamber is wet-cleaned. After cleaning, the work flow is repeated from step a).

As previously mentioned, using Exelan as the etcher greatly reduces the frequency for cleaning. A certain factory was able to use Exelan for oxide etching for 90 consecutive days without cleaning [12]. With Exelan, Lam Research made a breakthrough and altered the common sense in oxide dry etching that had been practised for over fifteen years. This breakthrough provides an explanation for the soaring of Lam Research Japan's market share for oxide etchers. Lam Research Japan has made an innovation in oxide dry etching technology.

7. Why Lam Research was able to achieve the innovation

What made Lam Research's innovation possible? This section studies Lam Research's corporate policy as grounds for their innovation.

What kind of corporate policy does Lam Research have? Lam Research's website (in English) states its mission as follows [18].

> 'Lam Research is dedicated to ***the success of our customers*** by being a world-class provider of ***innovative productivity solutions*** to the semiconductor industry. (Italics and bold by the author)'

As can be noted from this statement, an innovation-oriented culture is evident in Lam Research from its start-up days. This is a big difference from its competitors. What then, served as the driving force behind the innovation?

First, Lam Research was established in the United States in 1980. Their main business has been dry etcher, though they have also dealt with chemical mechanical polishing (CMP) and chemical vapour deposition (CVD) equipments in the past. What is distinctive is that Lam Research is currently the only manufacturer in the world specialising in the dry etcher business. On the contrary, TEL and Applied Materials cover a variety of semiconductor equipments as their business.

Second, the technology development policy of Lam Research. Lam Research founded an R&D centre in Silicon Valley in 1994. It has conducted many joint projects with academic institutions and universities. It can be said that Lam Research has an R&D-oriented culture. It should be emphasized that researchers from semiconductor manufacturers have played key roles in R&D for more than ten years at such R&D facilities. This history made possible the birth of a new oxide dry etching technology in which plasma does not touch the inner walls of the chamber, which is the foundation for Lam Research's remarkable innovation.

Third, the technical marketing strategy must be mentioned. Japanese firms traditionally have not been strong in their marketing strategies. Semiconductor equipment manufacturers are no exceptions. When quality and performance were the only and absolute criteria for competition, marketing strategies may not have mattered so much. But today, good products do not necessarily guarantee good sales. In particular, a sensitive technical marketing becomes critical in realizing an innovation.

Lam Research Japan seems to have put forth a full effort into technical marketing.

Their intention is indicated by Kazuo Nojiri, an ex-employee of a large semiconductor manufacturer (Hitachi) and the current managing director and CTO of Lam Research Japan, being appointed as the chief of technical marketing. In his Hitachi days, Nojiri was a world-famous dry etching engineer. From early on in the stage, Lam Research Japan investigated the technological trends and needs of semiconductor manufactures, and used these findings in deciding that they will be selling Exelan as an oxide etcher for 12-inch wafers and Cu/Low-k.

Innovation is defined as 'a merger of invention and insight leading to creation of social and economic values' [19]. Lam Research intensified the development of dry etching technology at R&D centres where the basics matter, and succeeded in developing an innovative oxide dry etcher. Lam Research gathered information, established a logical marketing strategy and put forth a full effort into technical marketing. As a result, Lam Research was able to achieve an innovation in the Japanese oxide etcher market.

Notes and References:

[1] Personal experiences conducted by the author working at Hitachi.

[2] Figures 1 and 2 are drawn by the author based on '*Semiconductor equipment data book*' (Electronic Journal, 1995-2004). Data for 2004 is employed from reference [3].

[3] Interview conducted by the author with an employee of Press Journal. Aug. 2005.

[4] Cu means copper wiring, and low-k means dielectric film with low relative dielectric constant. This is detailed in section 3.3.

[5] Interview conducted by the author with two engineers to semiconductor manufacturers in February 2005.

[6] Takuo Sugano (1980) *'Handoutai plasma process gijyutu (Semiconductor plasma process technology)'*, Tokyo, Sangyo-tosyo.

[7] Shinji Okazaki, Akiyosi Suzuki and Takumi Ueno (2003) '*Hajimeteno handotai lithography gijutsu (Semiconductor lithography technology for beginners)*', Tokyo, Kogyo Chosa-kai.

[8] Electronic Journal (2002) '2002 *Handotai technology taizen (2002 Semiconductor technology almanac)*'

[9] Kazuo Maeda (2004) '*Hajimeteno handotai nano-process (Semiconductor nano process for beginners)*', Tokyo, Kogyo chosa-kai.

[10] Kazuo Nojiri (2004) 'Lam Research no 65-45 nm taio dual-damacene etching gijutu (Lam Research dual-damascene etching technology for 65-45 nm node)', *Electric Journal Seminar*, Fig.2.

[11] Eric A. Hudson et al, (2003) **"**Control of Line Edge Roughness for Etching with 193nm Photoresist" Dry Process Symposium, p.253.

[12] Interview conducted by the author with two engineers at Japanese semiconductor manufacturers in Feb. 2005.

[13] Personal experiences conducted by the author working at Elpida Memory Inc., Semiconductor Leading Edge Technologies, Inc. (Selete), in 2000-2002

[14] Interview conducted by the author with Mr. Masayuki "Mike" Morita, President of Lam Research Japan, in Dec. 2005.

[15] Interview conducted by the author with an engineer at Japanese semiconductor manufacturers in Aug. 2005.

[16] Interview conducted by the author with an engineer at Japanese semiconductor manufacturers in Sept. 2005.

[17] Personal experiences conducted by the author working at Hitachi. 1995-2000.

[18] Lam Research Home Page, Company, Strategy, Mission.Vision.Value, http://www.lamresearch.com/main.cfm?section=1&subsection=3&subsubsection=4&subnav=subnav_1.cfm&contenturl=company_3_4.htm

[19] Council on Competitiveness (2004),*"Innovate America: Thriving in a World of Challenge and Change-National Innovation Initiative Summit & Report"*.